AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-12. (Canceled)

13. (Currently Amended) A semiconductor device package, comprising:

a semiconductor device, said device having been provided with points of electrical contact in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps, said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal, said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device wherein said pillar metal comprises two metal layers, and wherein said solder bumps extend over said pillar metal by at least 0.2 microns;

a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a

second surface thereof, said points of electrical contact provided over the second surface of said BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate;

a solder mask provided over said second surface of said BGA substrate;

said device being positioned over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate;

electrical contact having been established between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow;

said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device;

contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate; and

electrical contact having been established between said solder balls inserted into said solder mask provided over said

first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

14. (Original) The semiconductor device package of claim 13, said solder mask provided over said second surface of said BGA substrate being removed from said points of electrical contact provided over the second surface of said BGA substrate by a measurable amount, creating a channel through which cleaning solution can readily flow.

15. (Original) The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a peripheral pad design.

16. (Original) The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a center type pad design.

17. (Original) The semiconductor device package of claim 16, dummy solder bumps having been provided over the active surface of said device, providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine

pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

18. (Original) The semiconductor device package of claim 13, said fine pitch, high reliability solder bumps provided to said device comprising:

a layer of dielectric deposited over the active surface of said device, openings having been created in said layer of dielectric in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of passivation deposited over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device, openings having been created in said layer of passivation in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of metal barrier deposited over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device;

pillar metal and solder bumps overlying said layer of barrier metal in a pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and

said layer of barrier metal having been etched.

19. (Original) The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal.

20. (Original) The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal while further leaving in place said barrier layer extending from said pillar metal by a measurable amount.

21. (Original) The semiconductor device package of claim 13, said points of electrical contact in an active surface of said device having a pitch of about 200 μm or less.

22. (Original) The semiconductor device package of claim 13, flux removal from a gap between said second surface of said BGA substrate and said active surface of said semiconductor device having been performed after completion of flip chip assembly and solder reflow.

23. (Original) The semiconductor device package of claim 13, said encapsulation of said semiconductor device in a molding compound being replaced with an underfill for said device.

24. (Original) The semiconductor device package of claim 13, said height of columns of pillar metal being between about 10 and 100 μm and more preferably about 50 μm.